BER Improvement in the Zero-IF Receivers

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Abstract

The double balanced mixer scheme in-phase signal input and double-quadrature Local Oscillator is suggested for application on IQ direct conversion receivers. LO leakage influence on DC component and BER of the digital signal is shown. A model of the system is designed which is illustrating the improvement of the receiver sensitivity in case of using the suggested scheme.

1. Introduction

The increasing interest in the direct conversion or zero-IF receiver architecture (DCR) is based on several qualities of this type of reception which makes it very suitable for integration as well as multi-band multi-standard operation [1]. The main advantage of DCR, contrary to the most widely used heterodyne reception, is an achievement of high image rejection, which avoids the usage of expensive bulky off-chip filters. Among the problems existing in DCR, limiting their wide application, DC offset is one of the most serious.

To solve this problem the low-IF single conversion receiver architecture was proposed. Unfortunately, the low-IF receivers have comparatively insufficient suppression of an adjacent channel, especially in case of I/Q imbalance [2].

An alternative way of the DC problem solution is design of the DCR structures, where high LO-RF isolation is achieved [3].

DC offset caused by various phenomena contribute to the creation of DC signals. These phenomena can be separated on the three main groups, such as a) LO leakage to the LNA and mixers input due to substrate coupling, ground bounds, bond wire radiation etc., b) LO leakage to the antenna through the mixers and LNA due to their non-sufficient isolation, c) even-order nonlinearities of the LNA and mixer. The strength of DC caused by the phenomena of group a) is influenced by chip technology and can be reduced by careful layout or by suitable post processing digital signal processing (DSP) at baseband. DSP removes the DC offset in a way that using cannot be duplicated in the analog domain. For the cases of DC caused by the phenomena of groups b) and c) reductions in DC signal can be achieved in the analog domain by special circuit design [4]. This paper presents one such circuit.

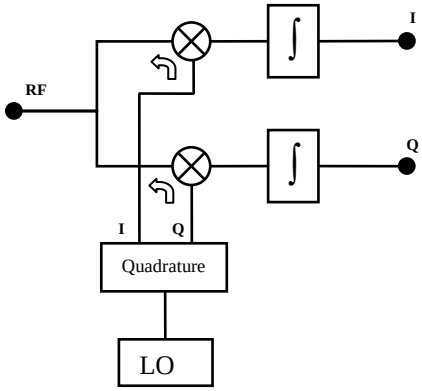

Figure 1. Direct conversion receiver

2. Four-quadrant multiplier DCR

The basic diagram of the conventional IQ DCR is given in Fig. 1. The possible DC offset due to LO self-mixing can be estimated using LO level in the mixers, LO-to-RF isolation and reflection from the RF interface mismatch. Taking into account the typical value for LO-to-RF isolation of the mixer -20dB, reverse gain of the LNA -20 dB, corresponding to mismatch SWR=1.1 reflection -20 dB and required LO level approximately 0 dBm, the LO leakage -60 dBm at the LNA input can be obtained. This value of LO leakage power is 30 dB higher than required sensitivity threshold of the receiver. Leakage power after amplification of LNA and self-mixing with LO produces a DC offset on the order of 10 mV at the output of the mixer, which is high enough to saturate the following circuits.

To solve this kind of DC offset problem various compensative and balanced architectures have been suggested [1], [5]. To reduce the LO leakage and DC offset we suggest to use the scheme of analogue double balanced mixers presented in Fig. 2. As distinct from well known scheme with double-quadrature division of input RF and LO [6], here we use in-phase division of RF and quadrature-antiphase

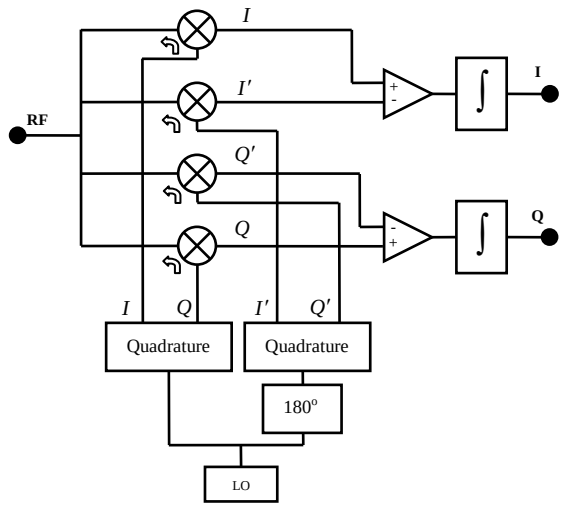

Figure 2. Double balanced DCR

division of LO. Such construction allows to suppress LO leakage to the front end, because at the entry of in-phase splitter the two equal antiphase components have been summed. Presence of differential pairs (I,I') and (Q,Q') enables suppression of residual DC offsets at the I and Q outputs.

Double Quadrature LO generation is however a critical part of this system due to gain and phase mismatches. To find out the influence of the gain (Δ) and phase (Θ) mismatches on the behavior of this scheme let us write the LO signals as follows

$$LO_I = (1+\Delta_1)\cos(\omega_c t + \Theta_1) \quad (1a)$$

$$LO_{I'} = -(1-\Delta_1)\cos(\omega_c t - \Theta_1) \quad (1b)$$

$$LO_Q = (1+\Delta_2)\sin(\omega_c t + \Theta_2) \quad (1c)$$

$$LO_{Q'} = -(1-\Delta_2)\sin(\omega_c t - \Theta_2) \quad (1d)$$

Hence the LO leakage at RF port will be presented as

$$LO_L = L_R \cdot L_M \left(LO_I + LO_{I'} + LO_Q + LO_{Q'}\right) \quad (2)$$

The improvement of the LO leakage suppression (L_{4IQ}) in the suggested scheme compared to those in the non-balanced scheme (L_{IQ}) which was presented in Fig. 1 is shown in Fig. 3.

The output of the mixers after filtering of the double-frequency components are the following

$$I = \frac{1}{8}(1+\Delta_1)\left[a(t)\sin\Theta_1 + b(t)\cos\Theta_1\right] + DC_I \quad (3a)$$

$$I' = -\frac{1}{8}(1-\Delta_1)\left[-a(t)\sin\Theta_1 + b(t)\cos\Theta_1\right] + DC_{I'} \quad (3b)$$

$$Q = \frac{1}{8}(1+\Delta_2)\left[a(t)\cos\Theta_2 + b(t)\sin\Theta_2\right] + DC_Q \quad (3c)$$

$$Q' = -\frac{1}{8}(1-\Delta_2)\left[a(t)\cos\Theta_2 - b(t)\sin\Theta_2\right] + DC_{Q'} \quad (3d)$$

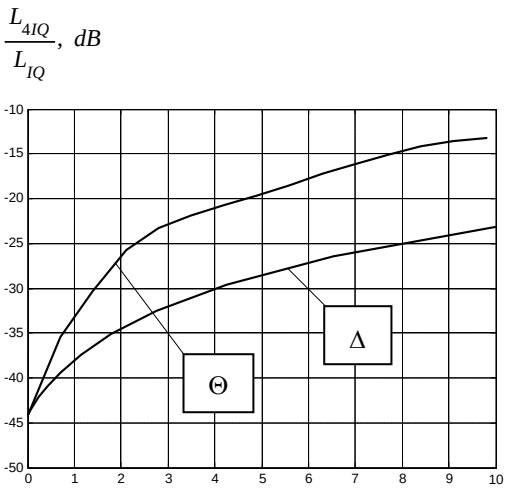

Figure 3. Leakage suppression at RF port in double balanced DCR

where DC_I, $DC_{I'}$, DC_Q, $DC_{Q'}$ are DC offsets at corresponding branches and can be calculated using (1) and (2). The improvement of the DC offset (DC_{4IQ}) in the suggested scheme compared to those in the non-balanced arrangement (DC_{IQ}) is shown in Fig. 4.

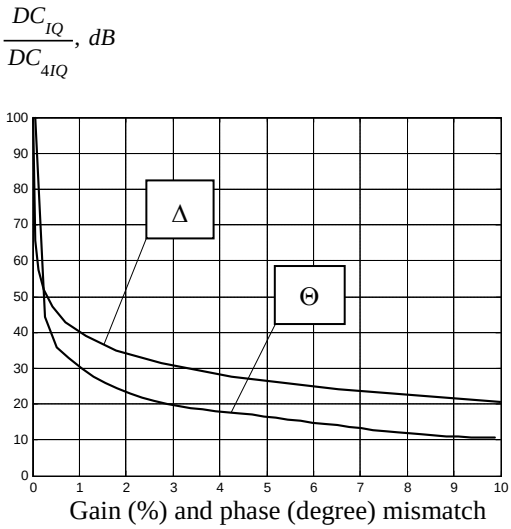

Figure 4. DC offset improvement in double balanced DCR against the gain and phase mismatch

As it can be seen from (3) I,I' and Q,Q' are represented as differential pairs. Hence the wanted signal can be obtained in the following way

$$I(t) = I - I'$$
$$Q(t) = Q - Q'.$$

The imbalance errors can be extracted as a sum of the I,I' and Q,Q' pairs

$$\varepsilon(I) = I + I'$$
$$\varepsilon(Q) = Q + Q'.$$

These values can be used for imbalance compensation at the source of the LO phase splitter, or digitally after A/D conversion.

As it is seen from the above discussion, LO leakage, DC offset and I/Q imbalance strongly depend on the gain and phase mismatches of the LO splitter. The use of a cascaded four-branch RC polyphase network [7] or polyphase oscillator [8] makes it possible to reach 0.5° phase error and 0.5 dB amplitude error. For such mismatches the suggested scheme provides LO leakage suppression at the RF input of more than 90 dB which is sufficient for many applications of DCR.

3. Digital link simulation model

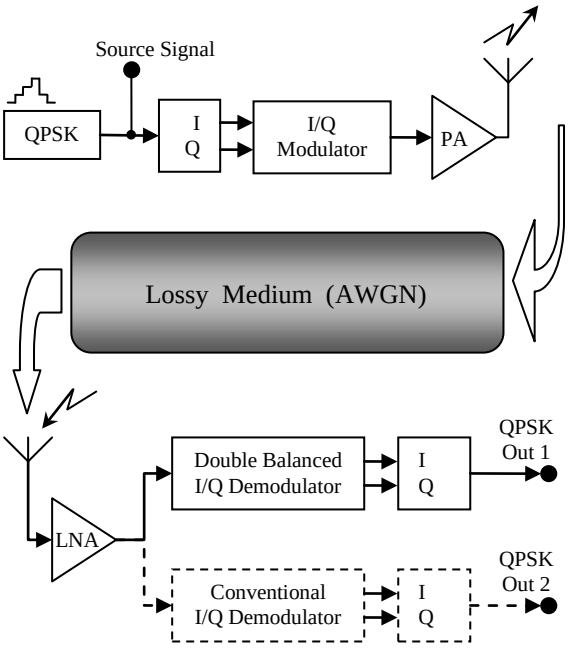

Figure 5. Block diagram of the QPSK digital link model

In the latest decades the major interest of the radio wave propagation is related to the wireless communication, especially the digital signal transmission and reception (cell phones, wireless computer network, satellite communication, military issues etc.). The main requirements for the digital transmitters/receivers are the possibility of easy integration with digital signal processing units, small size and simplicity.

A model in the Matlab 6.5 software environment is developed for the direct conversion receiver behavior consideration using well known QPSK signal for traditional and suggested schemes.

The block diagram of the model is shown in Fig. 5. Four-level baseband digital signal is being divided into two binary streams. These streams are connected to the I and Q entries of the digital I/Q modulator.

Modulated and propagated signal is being passed through the noisy channel simulator. After receiving it was amplified by the low noise amplifier and demodulated separately by double balanced receiver and conventional I/Q direct conversion receiver. There are integrators in the demodulator blocks (see Fig. 1 and Fig. 2), one per each of I and Q channels, which are accumulating the energy during one bit duration, comparing it with the neutral value and giving the decided value of the demodulated bit. Then two binary streams are combined into one four-level stream.

The outputs of the double balanced and conventional demodulators are being compared with initial source signal to determine the error rate of detected symbol streams. SER calculator block compares each received symbol with original one and in case of mismatch increments its internal error counter. The output of SER calculator block is the ratio of error count and the count of the total symbols received.

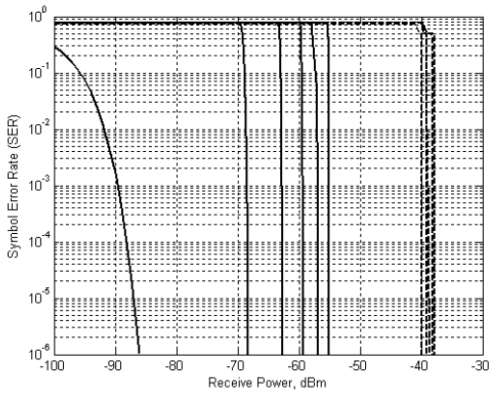

Figure 6. Symbol error rate dependencies from input signal power for the double balanced receiver (solid lines) and conventional receiver (dashed lines). Appropriate phase mismatches are 0, 1, 2, 3, 4, 5 degrees from left to right

4. Simulation results

The noise level of LNA was kept unchanged (E_s/N_0=10 dB, when input signal power equals -60 dBm), while the input signal power was varying within wide range for both receivers.

For the different phase mismatch values the dependency between received signal power and symbol error rate was computed and shown in Fig. 6.

In case of zero degree phase mismatches for the suggested scheme we have the first solid line from left and the first dashed line for the conventional DCR. As we can see the first curve is describing well known relationship between BER and signal power. Thus, even big LO leakage does not distort the characteristics of the receiver in case of ideal LO and phase shifters. Increasing the phase mismatch deforms this characteristics, and minimal required power of the signal grows up to -55 dBm i.e. the LO leakage becomes more essential.

On the other hand the behavior of the conventional DCR is much worse. The dependency of symbol error rate from signal power is steeply inclined and the sensitivity has a weak dependency from the phase mismatch.

Anyway, as we can note from Fig. 6, even in case of sufficient (5 degree) phase mismatch the dynamic range of the double balanced DCR is about 20 dBm higher compared with conventional one.

Assuming the acceptable symbol error rate 10^{-6} the minimum required signal power was calculated for different phase mismatches. The dependency between the phase mismatch and required power level is shown in Fig. 7.

The slope of the curve for double balanced DCR is sufficient when the phase mismatch is little and it

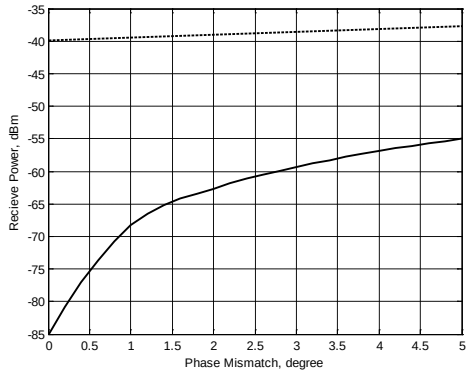

Figure 7. Receiver sensitivity dependencies from phase mismatch in case of fixed acceptable SER=10^{-6} for double balanced DCR (solid line) and conventional receiver (dashed line)

becomes less growing when the mismatch is high.

As we can note again from Fig. 7 the sensitivity of the double balanced receiver is much higher compared with conventional one even in case of significant phase imbalance. However, in case of 0.5 degree phase mismatch we have about 35 dB of sensitivity improvement.

5. Conclusions

The usage of suggested double balanced mixer in the direct conversion receivers results DC offset suppression and therefore increased sensitivity and dynamic range of whole receiver. This technique is quite simple and has low cost. It can be realized within one integral circuit. Based on the cost and performance analysis, it is believed that there will be a number of successful applications of this technique, especially to design transceivers for the systems like GSM, Bluetooth and 3G/4G wireless networks.

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